Fig. 1

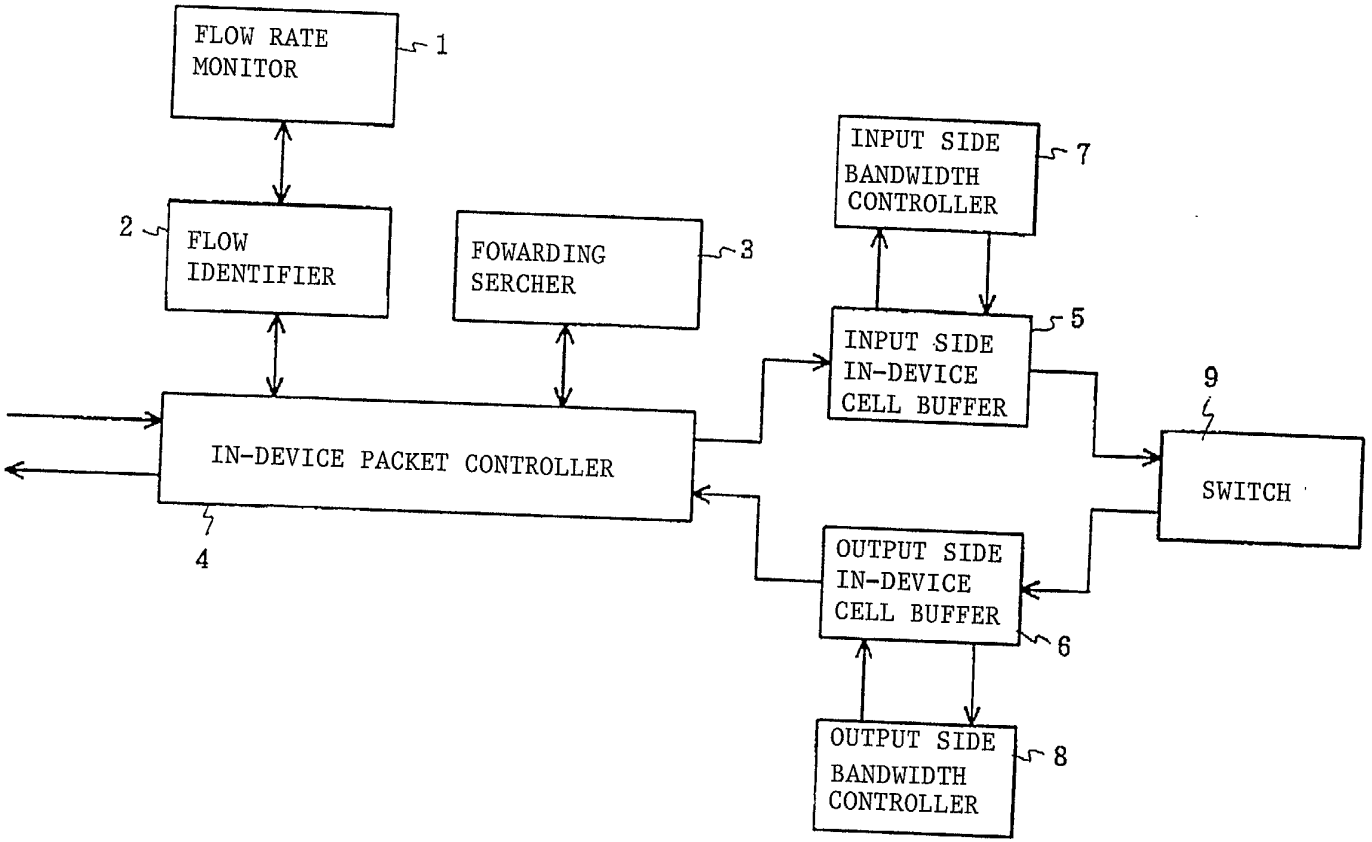

FLOW RATE MONITOR
1
2
FLOW IDENTIFIER
FOWARDING SERCHER
3
INPUT SIDE BANDWIDTH CONTROLLER
7
INPUT SIDE IN-DEVICE CELL BUFFER
5
9
SWITCH
IN-DEVICE PACKET CONTROLLER
4
OUTPUT SIDE IN-DEVICE CELL BUFFER
6
OUTPUT SIDE BANDWIDTH CONTROLLER
8

Fig. 2

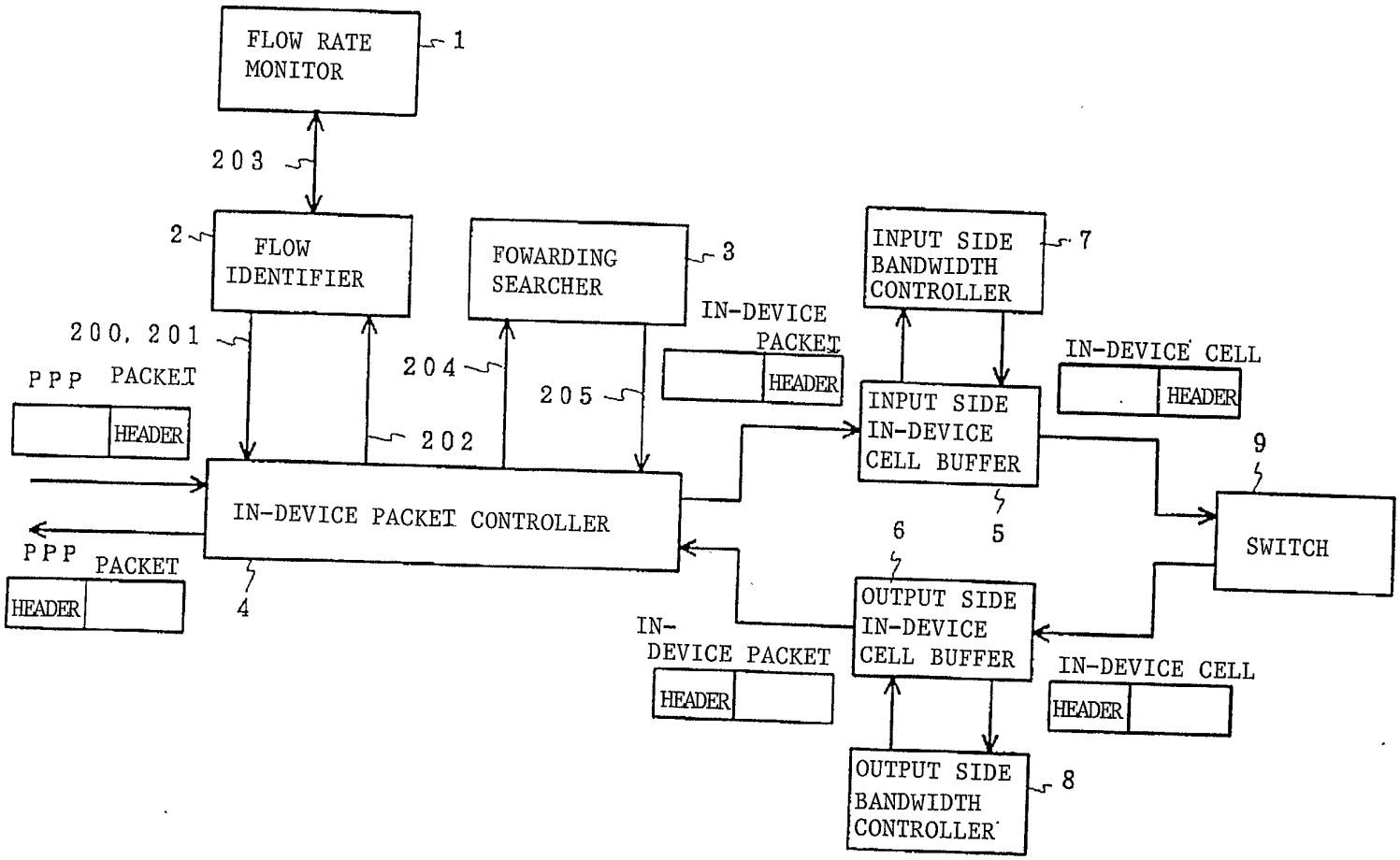

FLOW RATE MONITOR
1
203
2
FLOW IDENTIFIER
FOWARDING SEARCHER
3
INPUT SIDE BANDWIDTH CONTROLLER
7
IN-DEVICE PACKET
HEADER
IN-DEVICE CELL
HEADER
200, 201
PPP PACKET
HEADER
204
205
202
INPUT SIDE IN-DEVICE CELL BUFFER
5
9
SWITCH
IN-DEVICE PACKET CONTROLLER
6
PPP PACKET
HEADER
4
OUTPUT SIDE IN-DEVICE CELL BUFFER
IN-DEVICE PACKET
HEADER
IN-DEVICE CELL
HEADER
OUTPUT SIDE BANDWIDTH CONTROLLER
8

Fig. 3

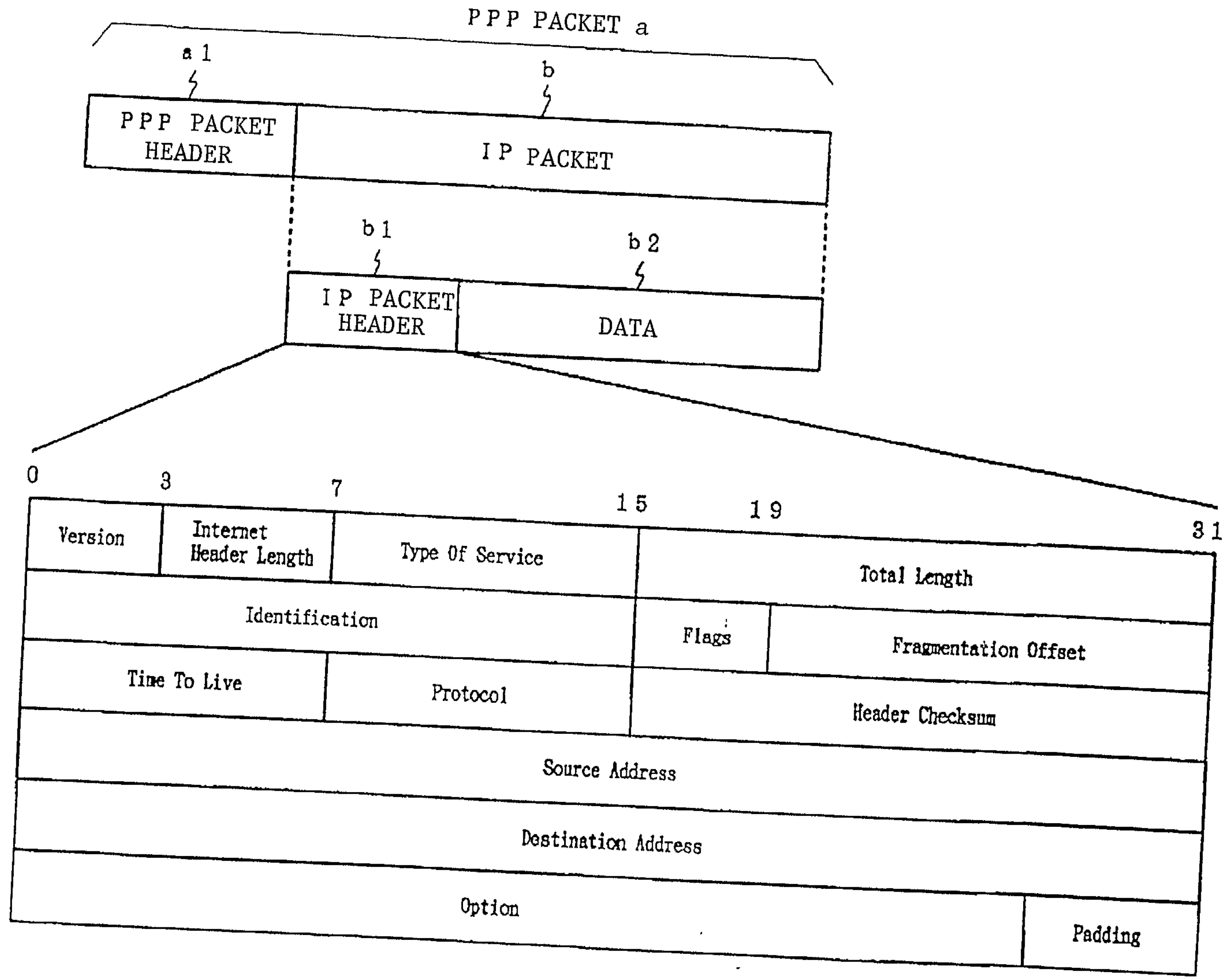

PPP PACKET a
a1
b
PPP PACKET HEADER
IP PACKET
b1
b2
IP PACKET HEADER
DATA
0
3
7
15
19
31
Version
Internet Header Length
Type Of Service
Total Length
Identification
Flags
Fragmentation Offset
Time To Live
Protocol
Header Checksum
Source Address
Destination Address
Option
Padding

Fig. 4

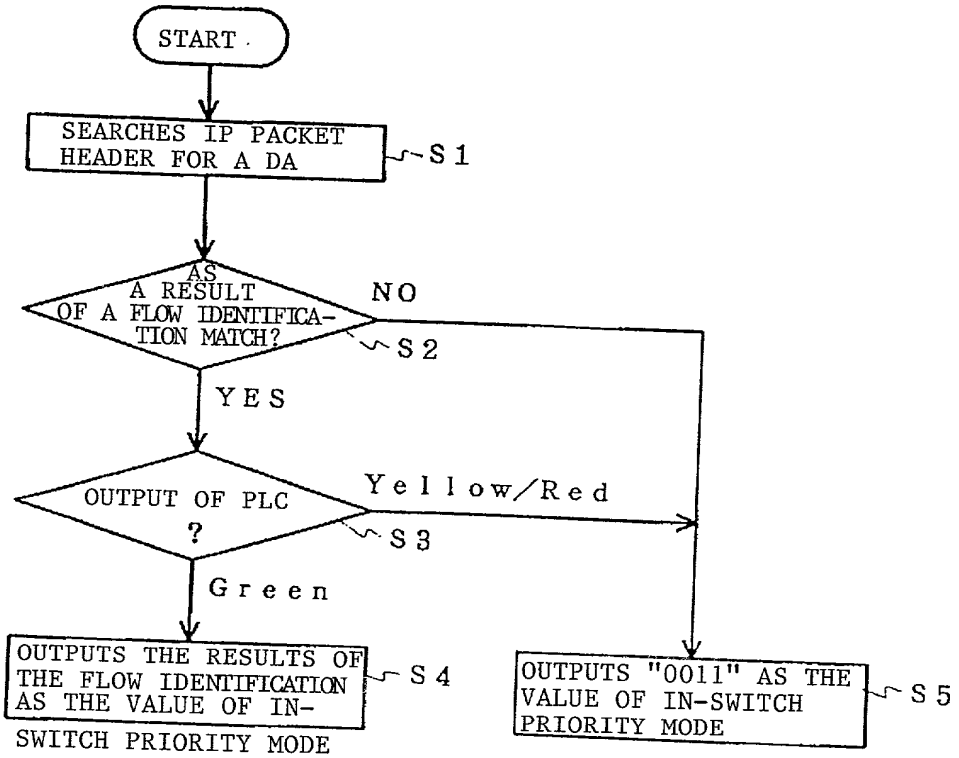

START
SEARCHES IP PACKET HEADER FOR A DA
S1
AS A RESULT OF A FLOW IDENTIFICATION MATCH?
NO
S2
YES
OUTPUT OF PLC ?
Yellow/Red
S3
Green
OUTPUTS THE RESULTS OF THE FLOW IDENTIFICATION AS THE VALUE OF IN-SWITCH PRIORITY MODE
S4
OUTPUTS "0011" AS THE VALUE OF IN-SWITCH PRIORITY MODE
S5

Fig. 5

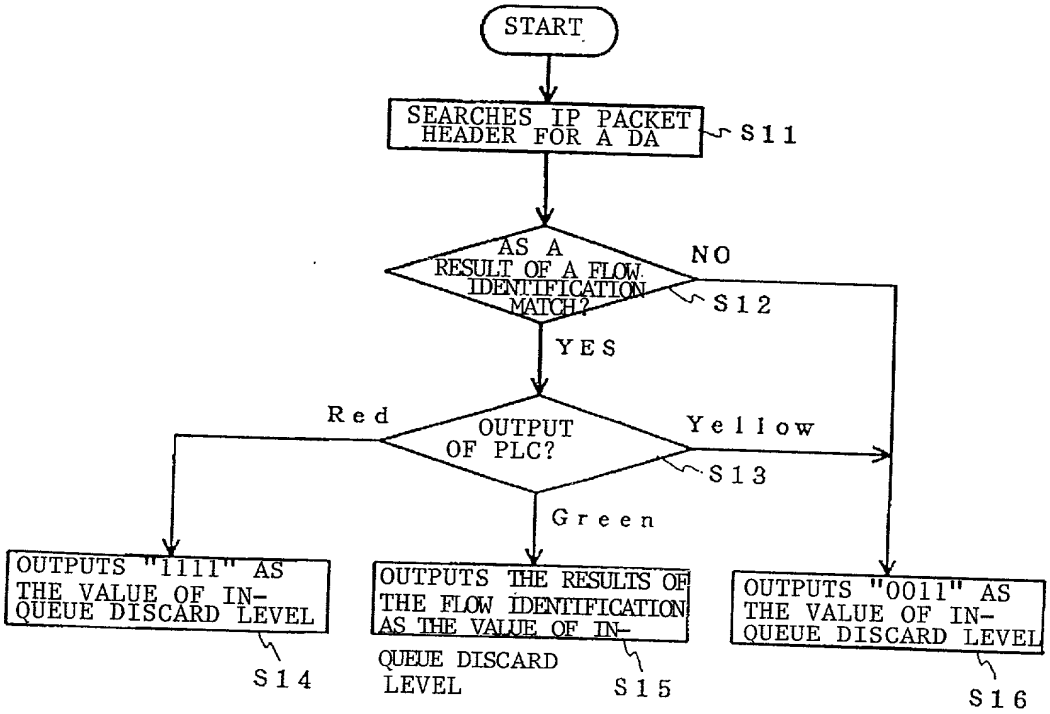

START
SEARCHES IP PACKET HEADER FOR A DA
S11
AS A RESULT OF A FLOW IDENTIFICATION MATCH?
NO
S12
YES
OUTPUT OF PLC?
Red
Yellow
Green
S13
OUTPUTS "1111" AS THE VALUE OF IN-QUEUE DISCARD LEVEL
S14
OUTPUTS THE RESULTS OF THE FLOW IDENTIFICATION AS THE VALUE OF IN-QUEUE DISCARD LEVEL
S15
OUTPUTS "0011" AS THE VALUE OF IN-QUEUE DISCARD LEVEL
S16

Fig. 6

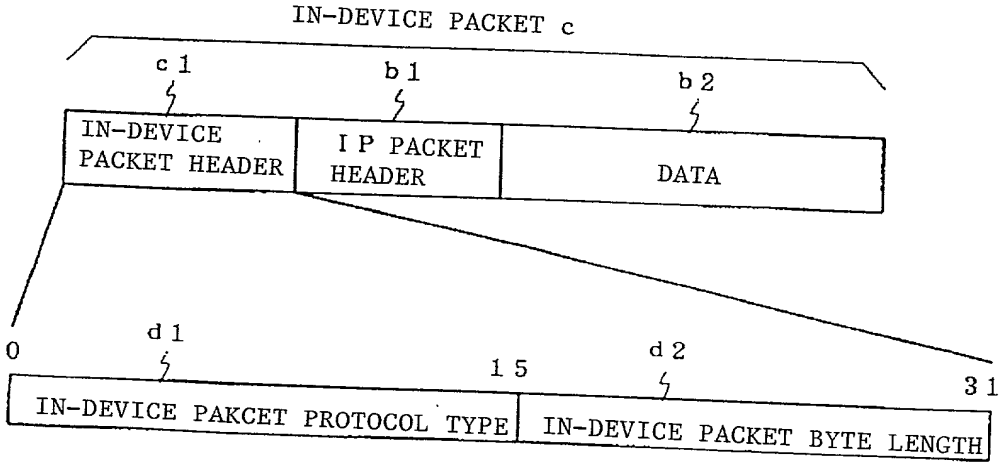

IN-DEVICE PACKET c
c1
b1
b2
IN-DEVICE PACKET HEADER
IP PACKET HEADER
DATA
0
d1
15
d2
31
IN-DEVICE PAKCET PROTOCOL TYPE
IN-DEVICE PACKET BYTE LENGTH

Fig. 7

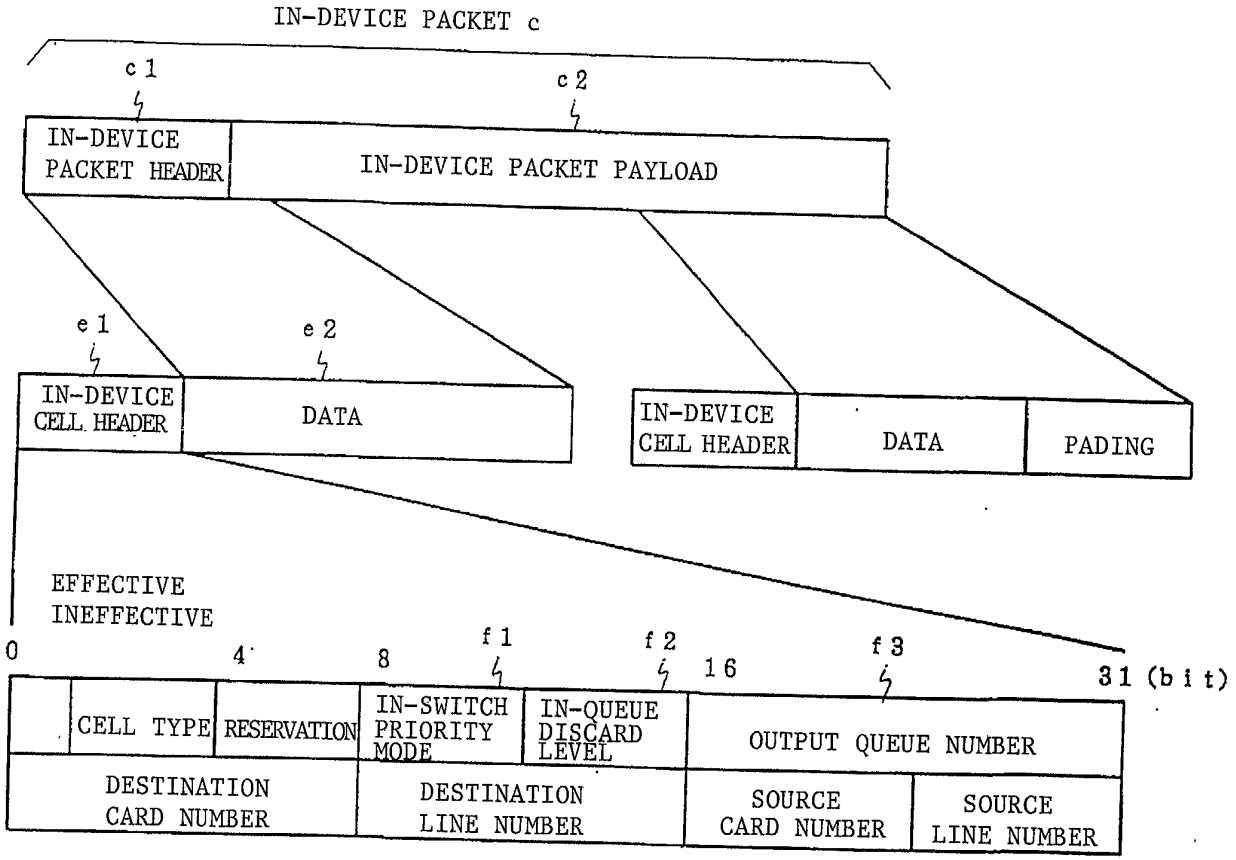

IN-DEVICE PACKET c
c1
c2
IN-DEVICE PACKET HEADER
IN-DEVICE PACKET PAYLOAD
e1
e2
IN-DEVICE CELL HEADER
DATA
IN-DEVICE CELL HEADER
DATA
PADING
EFFECTIVE
INEFFECTIVE
0
4
8
f1
f2
16
f3
31 (bit)
CELL TYPE
RESERVATION
IN-SWITCH PRIORITY MODE
IN-QUEUE DISCARD LEVEL
OUTPUT QUEUE NUMBER
DESTINATION CARD NUMBER
DESTINATION LINE NUMBER
SOURCE CARD NUMBER
SOURCE LINE NUMBER

Fig. 8

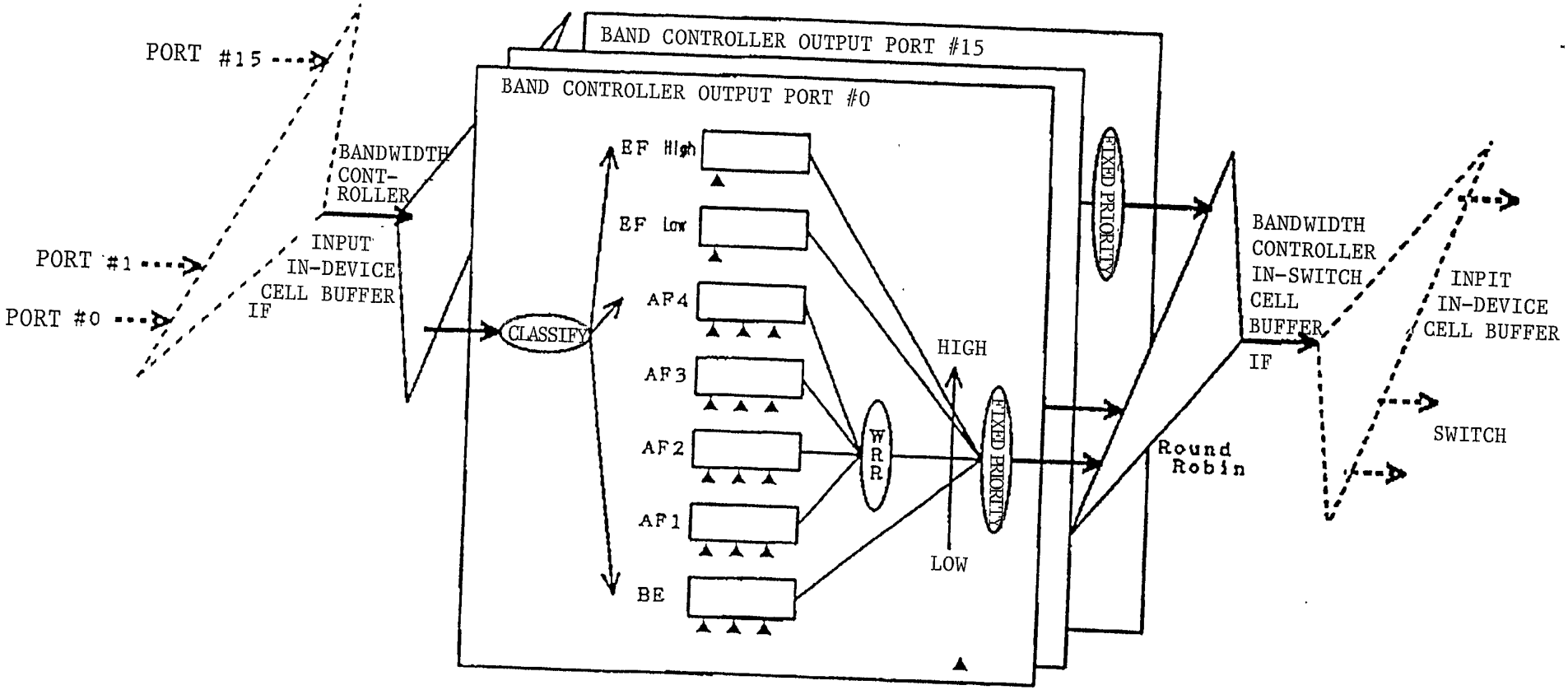

PORT #15
PORT #1
PORT #0
BANDWIDTH CONT-ROLLER
INPUT IN-DEVICE CELL BUFFER IF
CLASSIFY
BAND CONTROLLER OUTPUT PORT #15
BAND CONTROLLER OUTPUT PORT #0
EF High
EF Low
AF4
AF3
AF2
AF1
BE
WRR
HIGH
LOW
FIXED PRIORITY
FIXED PRIORITY
BANDWIDTH CONTROLLER IN-SWITCH CELL BUFFER IF
Round Robin
INPIT IN-DEVICE CELL BUFFER
SWITCH

Fig. 9

IN-SWITCH PRIORITY MODE	PRIORITY MODE	OUTPUT SIDE IN-DEVICE CELL BUFFER	INPUT SIDE IN-DEVICE CELL BUFFER	REMARKS
XX00	HIGHEST PRIORITY	EF (H)	EF	WITH DELAY ASSURANCE
XX01	SECOND HIGHEST PRIPRITY	EF (L)		WITH BANDWIDTH ASSURANCE
0010	THIRD HIGHEST PRIORITY	AF1	AF1	WITH DELAY ASSURANCE
0110	"	AF2	AF2	
1010	"	AF3	AF3	WITHOUT BANDWIDTH ASSURANCE
1110	"	AF4	AF4	
XX11	LEAST HIGIEST PRIORITY	BE	BE	WITHOUT DELAY ASSURANCE WITHOUT BANDWIDTH ASSURANCE

Fig. 10

VALUE OF IN-QUEUE DISCARD LEVEL	DISCARD PRIORITY IN BANDWIDTH CONTROLLER
0000	LOW DISCARD PROBABILITY ↓ ↓ HIGH DISCARD PROBABILITY
0001	
0010	
0011	
1111	WITHOUT FAIL IN IN-DEVICE PACKET CONTROLLER

Fig. 11

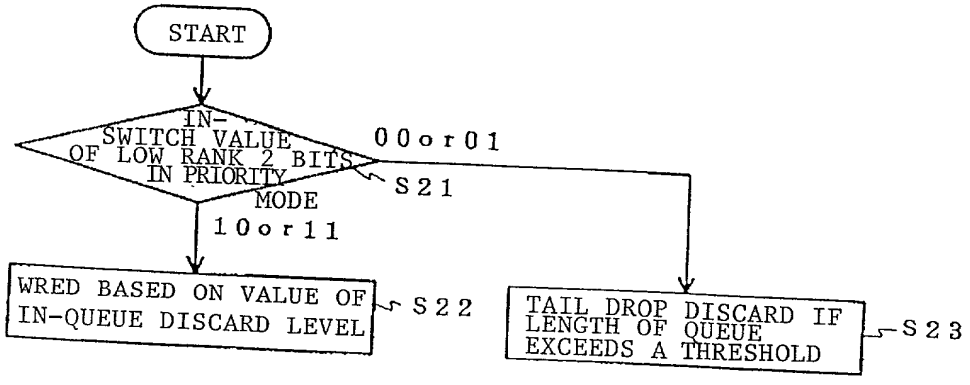


Fig. 12

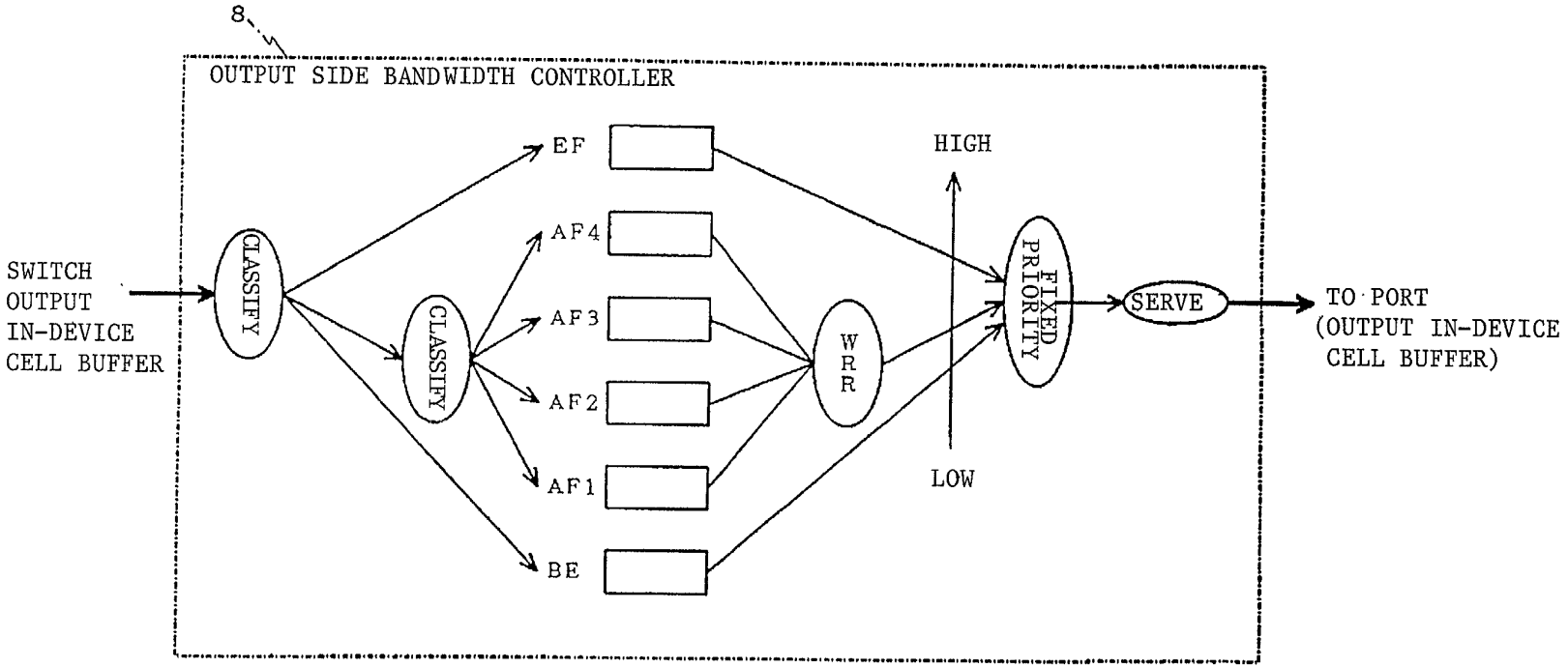

8
OUTPUT SIDE BANDWIDTH CONTROLLER
SWITCH OUTPUT IN-DEVICE CELL BUFFER
CLASSIFY
CLASSIFY
EF
AF4
AF3
AF2
AF1
BE
WRR
HIGH
LOW
FIXED PRIORITY
SERVE
TO PORT (OUTPUT IN-DEVICE CELL BUFFER)

Fig. 13

	IN-QUEUE NUMBER		
	INPUT SIDE IN-DEVICE CELL BUFFER MODE	OUTPUT SIDE IN-DEVICE CELL BUFFER MODE	
XX00	112 ~127	96 or 112	SIMPLE PRIORITY QUEUE 1 (CORRESPOND TO DIFF SERV EF CLASS) EF(H)
XX01	96~111		SIMPLE PRIORITY QUEUE 1 (CORRESPOND TO DIFF SERV EF CLASS) EF(L)
0010	16~31	16	WRR QUEUE 1 (DIFF SERV AF1 CLASS)
0110	32~47	32	WRR QUEUE 2 (DIFF SERV AF1 CLASS)
1010	48~63	48	" 3 (")
1110	64~79	64	" 4 (")
XX11	00~15	0	BE QUEUE (BE CLASS)

Fig. 14

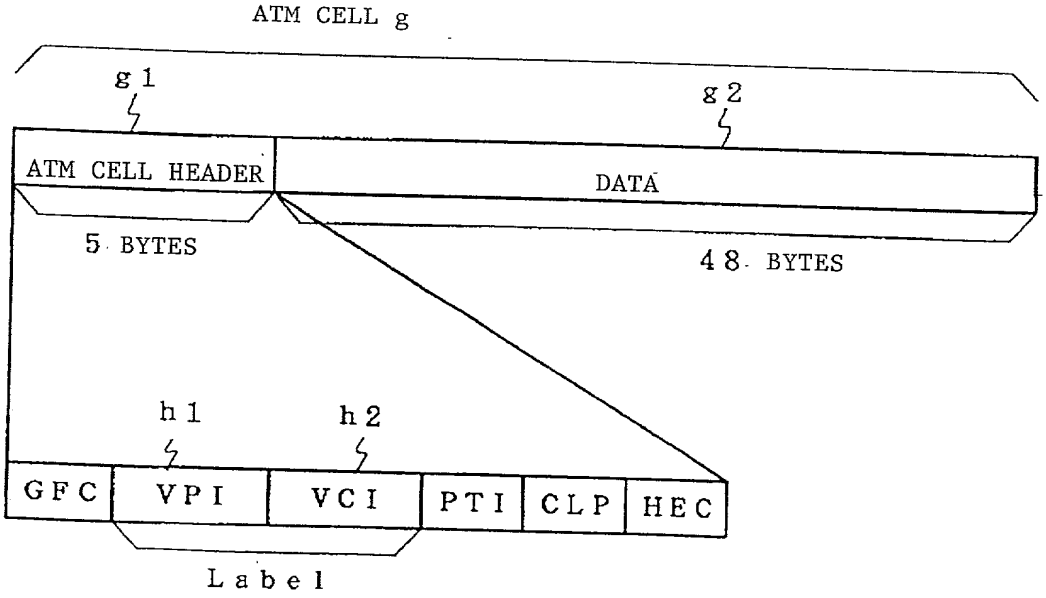


Fig. 15

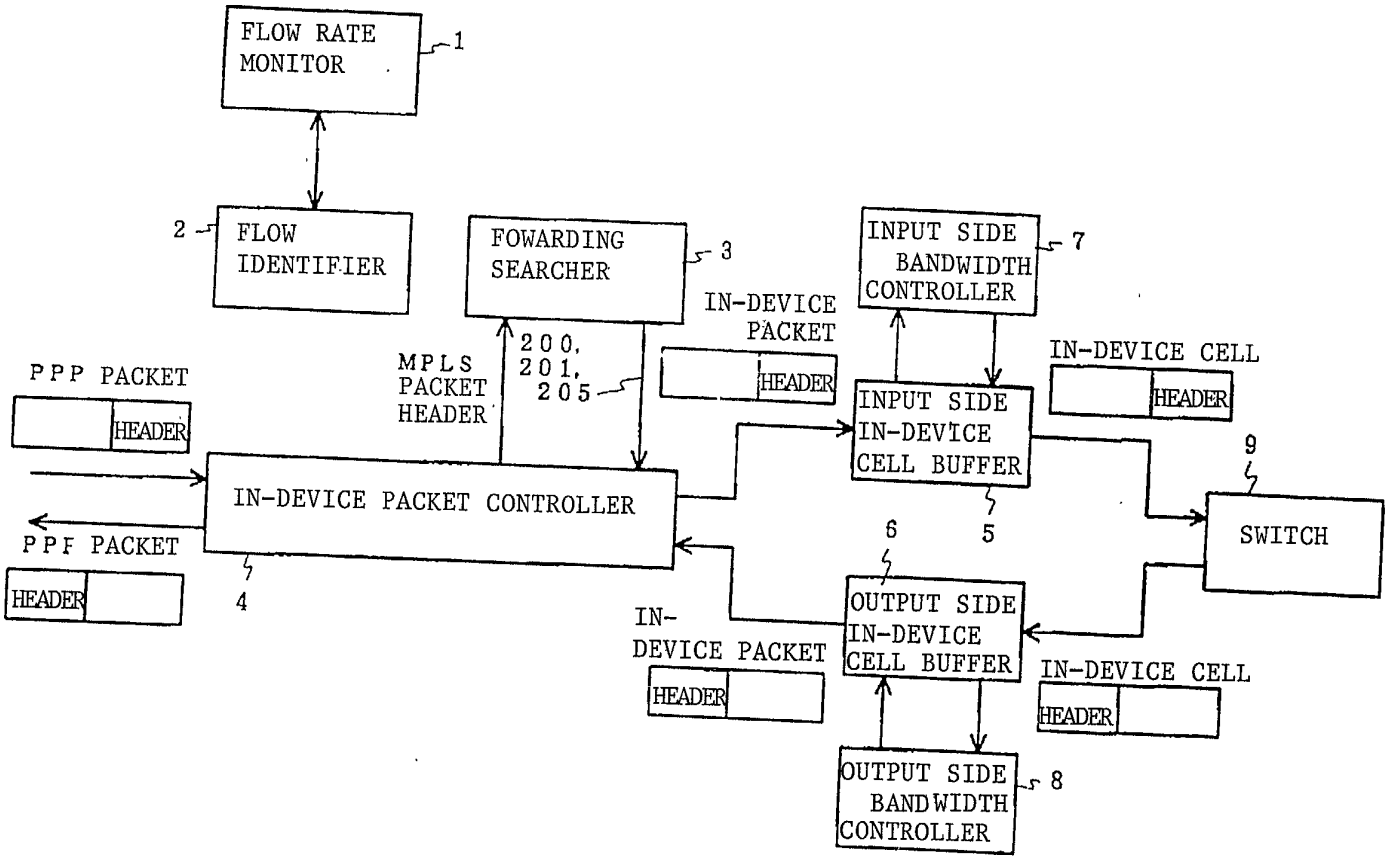
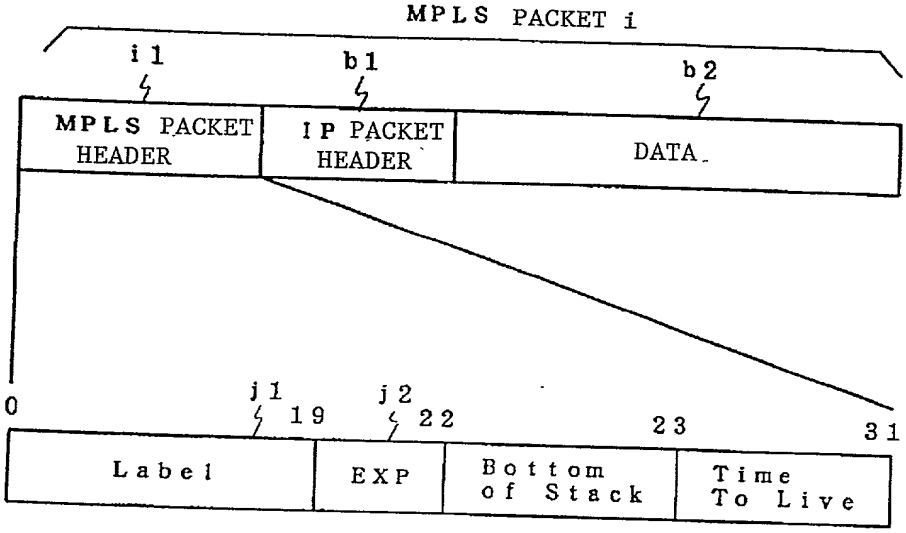

FLOW RATE MONITOR
1
2
FLOW IDENTIFIER
FOWARDING SEARCHER
3
INPUT SIDE BANDWIDTH CONTROLLER
7
IN-DEVICE PACKET
HEADER
IN-DEVICE CELL
HEADER
PPP PACKET
HEADER
MPLS PACKET HEADER
200, 201, 205
INPUT SIDE IN-DEVICE CELL BUFFER
9
IN-DEVICE PACKET CONTROLLER
SWITCH
6
5
PPF PACKET
HEADER
4
OUTPUT SIDE IN-DEVICE CELL BUFFER
IN-DEVICE PACKET
HEADER
IN-DEVICE CELL
HEADER
OUTPUT SIDE BANDWIDTH CONTROLLER
8

Fig. 16


MPLS PACKET i
i1
b1
b2
MPLS PACKET HEADER
IP PACKET HEADER
DATA
0
j1
19
j2
22
23
31
Label
EXP
Bottom of Stack
Time To Live